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2012 SEMINAR SERIES PRESENTS

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Department of Mechanical and Materials Engineering

Dr. Maxime Darnon

CNRS -French National Center for Scientific Research-
Laboratory of Technologies of Microelectronics
Grenoble, France

Plasma Etching in Microelectronics

Integrated circuits are taking a more and more important part in our every day lives thanks to the ever increasing circuit's performance. Cost reduction and performance improvement have been made possible by the constant downscaling of the devices dimension which requires the definition of ever-smaller patterns. Plasma etching has been used for years for the transfer of patterns, but is now facing new challenges due to the reduction of the dimension and to the variety of stacked materials that need to be patterned.

After reviewing the basics of plasma etching, we will describe the new challenges faced by plasma etching technologies for the fabrication of the most advanced building blocks of integrated circuits (transistors, interconnects, memories). We will especially focus on the modification of the materials when they are exposed to the etching plasma and on the specific issues related to the patterns definition at the nanometer scale.

Dr Maxime Darnon received his M. Sc. and Ph. D. from Grenoble University, France, in 2007. He worked then as a research engineer at IMEC, Leuven, Belgium, and as a Research Staff Member in the advanced plasma group of IBM Research in the T. J. Watson Research Center in Yorktown Heights, NY, USA. His work mostly focused on plasma processes for microelectronics interconnects. In 2009, he joined the CNRS as a researcher assigned to the Laboratory of Technologies of Microelectronics (LTM), where he works on new plasma processes for microelectronics applications.

Tuesday, February 21—3:30 pm
Room 110 Jorgensen Hall

Host:
Dr. Jung Yul Lim
Department of Mechanical and Materials Engineering

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