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Department of Electrical Engineering*

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### *Nanofabrication Challenges for the Next Decade*

In the coming decade and beyond, we will want to fabricate complex, heterogeneous, 3-dimensional structures, at nanoscale resolution, for the purpose of achieving high levels of functionality. The planar process, i.e, lithography followed by pattern transfer, is the only technique we have for deterministically inputting structural information at the micro and nanoscale. However, that process is limited in resolution, is fundamentally planar, and historically has been driven by the narrow set of requirements of integrated-circuit manufacturing. As a consequence of this focus on the semiconductor manufacturing, the tools available are inappropriate for many important applications in research and low-volume manufacturing, and their cost is inordinately high. I will describe an innovative approach to lithography that will open up new areas of research and customized manufacturing.

In the fabrication of 3D nanostructures we are pursuing an approach that consists of first patterning thin membranes using planar-fabrication, and then stacking them to form a final whole. This enables one to employ the full array of 2D planar-fabrication techniques to achieve high spatial-information density in any membrane layer. The pre-patterned membranes can be inspected for defects prior to assembly, thereby enhancing yield. The major challenges are how to reliably clean, align, stack and bond the membranes, and how to avoid in-plane stress-induced distortion. I'll report on the current status of this approach..

**Wednesday, April 4, 4:00 pm  
Room 136, Jorgensen Hall**

**Host:  
Dr. Yongfeng Lu  
Department of  
Electrical Engineering**

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